QUALIFICATION TEST REPORT

Wafer Process: PHEMT1
Drawing No.: 100487

CMD124
CMD131
CMD133
CMD134
CMD192
CMD192C5
CMD199
CMD200
CMD201
CMD201P5

1.0 Introduction

The definition of a qualification family, as defined by EIA/JESD47 Stress Driven Qualification of Integrated Circuits, is all devices that use the same wafer fabrication technology, wafer fabrication process and wafer fabrication site.

This qualification procedure is designed to satisfy the reliability requirements for a GaAs MMIC amplifier using Custom MMIC's PHEMT1 wafer process. The C2026 die has been chosen to qualify the PHEMT1 amplifier product line.

1.1 General Description

The C2026 chip is a GaAs MMIC 15 GHz dual driver amplifier which produces a gain of 15dB and a 1dB compression point of 20dBm. There are two completely separate amplifier circuits on each chip. The chip utilizes a GaAs PHEMT process and operates at a positive drain bias of +5V and a negative gate bias of -0.5V.

2.0 Summary of Results

All testing has been completed. The activation energy for the PHEMT1 process is 1.86 eV. Using 85°C as the maximum operating temperature for the device, the equivalent device hours for 77,000 hours at 118°C is calculated to be 7,931,000 hours. Using a Chi-Square confidence level of 90%, the failure rate is calculated to be 2.9×10^{-7} failures per hour or 290 FIT. Using a Chi-Square confidence level of 60%, the failure rate is calculated to be 1.15×10^{-7} failures per hour or 115 FIT.

Test	Qty In	Qty Out	Pass / Fail
Initial Electrical	77	77	Complete
Burn-in, 240 hours	77	77	Complete
Interim Electrical	77	77	Pass
HTOL, 1000 hours	77	77	Complete
Final Electrical	77	77	Pass
Bond Pull	10	10	Pass
Die Shear	10	10	Pass
SEM Inspection	10	10	Pass
Metal and Dielectric Thickness	10	10	Pass