Introduction

The CMDS PHEMT2 Process is an advanced depletion mode AlGaAs / InGaAs pHEMT technology with self aligned ohmic contacts, two level thick metal global interconnects with air bridges, MIM capacitors and substrate vias.

The definition of a qualification family, as defined by EIA/JESD47 Stress Driven Qualification of Integrated Circuits, is all devices that use the same wafer fabrication technology, wafer fabrication process and wafer fabrication site. This qualification report will outline the screening that was performed to satisfy the reliability requirements for a GaAs MMIC device using Custom MMIC’s PHEMT2 wafer process.

Wafer level, die level, and package level devices have been screened from this process. The test vehicle used for wafer level screening was the on-wafer process control monitor (PCM). Screening identified as die level was performed on foundry Standard Evaluation Circuits (SEC), and on the Custom MMIC P/N CMD193. Package level screening was performed on a foundry SMT device and the Custom MMIC P/N CMD132P3. Moisture Sensitivity Level and ESD Classification was performed on multiple Custom MMIC packaged products.

Qualification testing will consist of the following;

- **Wafer Level Reliability**
  - High Temperature Unbiased Bake
  - Autoclave, unbiased
  - Temperature Cycle

- **Die Level Reliability**
  - High Temperature Operating Life (HTOL)
  - Physical Attributes (Bond Pull, Die Shear, Metal Thickness, SEM Inspection)

- **Package Level Reliability**
  - High Temperature Operating Life (HTOL)
  - Autoclave, unbiased
  - Highly Accelerated Temperature and Humidity Stress Test (HAST)
  - Temperature Cycle
  - Thermal Shock
  - Moisture Sensitivity Level
  - ESD Classification
The test vehicle for wafer level reliability screening was the foundry on-wafer process control monitor (PCM) structures. The PCM structures are representative of the various passive and active components manufactured with the pHEMT2 process. These structures include individual active devices, capacitors, various via and contact chains, leakage combs and other proprietary structures.

The test vehicle for die level reliability screening was a foundry Standard Evaluation Circuit, (SEC), and the Custom MMIC P/N CMD193.

The SEC was a group of discrete 480 um FETs (8 finger x 60 um wide fingers).

Custom MMIC P/N CMD193 is a GaAs MMIC, 8 GHz dual low noise amplifier which produces a gain of 21 dB and a noise figure of 1.4 dB, and operates at a positive drain bias of 3.6 V.

All screening identified as package level was performed on a foundry SMT device and the Custom MMIC CMD132P3.

The foundry packaged SMT device is a high linearity, very low noise, high gain pHEMT FET for general purpose, low noise front-end applications. Noise figures as low as 0.65 dB with gain of 12 dB at 12 GHz. The device is packaged in a plastic, 4 pin, MW-4 SMT package.

The CMD132P3 is a broadband MMIC low noise amplifier housed in a leadless 3x3 mm plastic surface mount package. The CMD132P3 is ideally suited for microwave radios and C and X-band applications where small size and low power consumption are needed. The broadband device delivers greater than 20 dB of gain with a corresponding output 1 dB compression point of +10 dBm and a noise figure of 1.4 dB. The CMD132P3 is a 50 ohm matched design eliminating the need for external DC blocks and RF port matching. The CMD132P3 amplifier is the perfect alternative to costly hybrid amplifiers.

Please refer to our product datasheet for more detailed device information on the CMD132P3.
Products Selected, cont’d

 CMD132P3, Plastic molded QFN 3x3 mm x 16 lead smt

 CMD132P3 Functional Block Diagram

Products Covered by this Process Qualification Report

| CMD119P3  | CMD161  | CMD173P4 | CMD193P3X4 | CMD221  |
| CMD132    | CMD162  | CMD185   | CMD194     | CMD222  |
| CMD132P3  | CMD163  | CMD185P3 | CMD194C3   | CMD223  |
| CMD157    | CMD163C4| CMD186P3 | CMD197     | CMD224  |
| CMD157P3  | CMD164  | CMD187   | CMD197C4   | CMD228  |
| CMD158    | CMD165  | CMD187C4 | CMD197P4   | CMD228P4|
| CMD158C4  | CMD166  | CMD188   | CMD202C5   | CMD229  |
| CMD158P3  | CMD167  | CMD188C4 | CMD205     | CMD229P4|
| CMD159    | CMD167P3| CMD189P3 | CMD205P3   |         |
| CMD160    | CMD168P3| CMD190   | CMD206     |         |
| CMD160C4  | CMD173  | CMD191C4 | CMD207     |         |
Process Qualification Report

CMDS PHEMT2 Wafer Process

High Temperature Wafer Bake, Unbiased

One wafer from each of three separate PHEMT2 lots, 70 PCM die on each wafer, were selected to go through a high temperature, unbiased bake. The wafers were baked at 275°C in air for 168 hours with data taken at the start, the middle, and the completion of the 168 hours. High Temperature bake is performed in air for acceleration of thermally activated failure mechanisms. A temperature of 275°C provides for maximum acceleration without compromising the dielectric material. This test is designed to simulate > 20 years of life at 150°C.

The PCM die were tested at the completion of the test and no degradation in performance was noticed.

Autoclave, Unbiased

One wafer from each of three separate PHEMT2 lots, 70 PCM die on each wafer, were selected to go through an unbiased autoclave. The wafers were stressed for 96 hours at 121°C and 100% relative humidity at 15 psia. The purpose of this test is to apply severe conditions of pressure, humidity, and temperature that accelerate the penetration of moisture into the wafer.

Electrical data was taken at the start and completion of the 96 hours, and no degradation in performance was noticed.

Temperature Cycle

One wafer from each of three separate PHEMT2 lots, 70 PCM die on each wafer, were selected to go through a temperature cycle performed according to JESD22-A104 Condition G. The wafers were subjected to 500 cycles of –40°C to +125°C in an effort to determine the resistance of a wafer to alternating extremes of high and low temperatures.

The PCM die were tested at the completion of the test and no degradation in performance was noticed.

Mean Time To Failure, Foundry SEC

Three separate groups of ten FETs each were packaged and stressed at three different temperatures until failure. The material was stressed at junction temperatures of 255°C, 270°C, and 285°C. The FETs were biased at a drain-source voltage of 3 V and at a drain-source current of 40 mA. Device failure was defined as when the operating current changed by 10% during the duration of the test.

◊ The deduced Activation energy for all 3 lots was 1.71eV.
◊ The projected MTTF at a Tj of 150°C is 1.2e7 hours.
Process Qualification Report

CMDS PHEMT2 Wafer Process

High Temperature Operating Life, CMD193

Ninety two CMD193 devices were subjected to a High Temperature Operating Life (HTOL) test screen. HTOL testing is used to determine the effect of bias and temperature on the device over an extended period of time. The material was subjected to 1000 hours at an ambient temperature that produced a junction temperature of 150°C once the device was biased at 3.6 V on the drain.

No degradation in device performance was noticed at the completion of the testing.

The CMD193 equivalent device hours is calculated to be 28,152,000 hours.

Using a Chi² distribution with a confidence level of 90% and 60%, the following FIT and MTTF are calculated:

\[ \lambda_{90\%} = 82 \text{ FIT and MTTF} = 1.22 \times 10^7 \text{ hours or 1,918 years} \]

\[ \lambda_{60\%} = 33 \text{ FIT and MTTF} = 3.03 \times 10^7 \text{ hours or 3,459 years} \]

Physical Attributes, CMD193

Destructive Bond Pull:
Ten die from one wafer were mounted to test coupons with conductive epoxy. Three wires on each of the ten die were thermo-sonically bonded from the die to the coupon. The bonded wires were then pulled to destruction in accordance with the requirements of MIL-STD-883, Method 2011, Condition C. No failures were found.

Destructive Die Shear:
The ten die used in the Destructive Bond Pull testing were subjected to die shear testing in accordance with MIL-STD-883, Method 2019. No failures were found.

Metal and Dielectric Thickness:
Ten die from one wafer were mounted, cross-sectioned and polished. Metal and dielectric thickness was recorded for each layer and compared to expected values. There were no anomalies found.

SEM Inspection:
Ten die from one wafer were mounted and sequentially delayered to perform SEM inspection to the requirements of MIL-STD-883 Method 2018. There were no anomalies found.
Process Qualification Report
CMDS PHEMT2 Wafer Process

**High Temperature Operating Life, MW-4 SMT**

Two groups of seventy seven packaged devices each were subjected to 1000 hours at an ambient temperature that generated a junction temperature of 150°C when biased at 3 V in order to determine the effect of bias and temperature on the device over an extended period of time. The devices were tested prior to and at completion of the HTOL screening. No degradation in product performance was noticed.

**High Temperature Operating Life, CMD132P3**

Eighty packaged devices were subjected to 1000 hours at an ambient temperature that generated a junction temperature of 150°C when biased at 3.6 V in order to determine the effect of bias and temperature on the device over an extended period of time. The devices were tested prior to and at completion of the HTOL screening. No degradation in product performance was noticed.

**Autoclave, unbiased, CMD132P3**

Seventy seven packaged devices were selected to go through an unbiased autoclave. The devices were stressed for 96 hours at 121°C and 100% relative humidity and at 29.7 psia. The purpose of this test is to apply severe conditions of pressure, humidity, and temperature that accelerate the penetration of moisture into the device. The material was tested at the start and completion of the 96 hours, and no degradation in performance was noticed.

**HAST, biased, CMD132P3**

Eighty packaged devices were selected to go through an unbiased autoclave. The devices were stressed for 96 hours at 130°C, 85% relative humidity, and biased at 3.6 V. The purpose of this test is to apply severe conditions of humidity, and temperature that accelerate the penetration of moisture into the device. The material was tested at the start and completion of the 96 hours, and no degradation in performance was noticed.
Process Qualification Report
CMDS PHEMT2 Wafer Process

Temperature Cycle, CMD132P3

Seventy seven packaged devices were selected to go through a temperature cycle performed according to JESD22-A104 Condition G. The devices were subjected to 1000 cycles of –40°C to +125°C in an effort to determine the resistance of the devices to alternating extremes of high and low temperatures. The ramp rate between extremes was 12.0°C/minute and the dwell time at each extreme was 15 minutes. The devices were tested at the completion of the test and no degradation in performance was noticed.

Thermal Shock, CMD132P3

Seventy seven packaged devices were subjected to a thermal shock performed according to JESD22-A106 Condition C. The devices were subjected to 100 cycles of –40°C to +125°C in an effort to determine the resistance of the devices to alternating extremes of high and low temperatures. The ramp rate between extremes was < 20 seconds and the dwell time at each extreme was 15 minutes. The devices were tested at the completion of the test and no degradation in performance was noticed.

Package Ass’y, Moisture Sensitivity Level Classification

Material samples from two non-consecutive build lots from three different part numbers were electrically tested before and after being subjected to the procedure specified in J-STD-020E, classification level MSL1. Visual inspection and acoustic microscope inspection (CSAM) was performed before and after moisture soak and reflow per MSL1 levels specified by IPC/JEDEC J-STD-020E. No degradation in product performance was seen.

All material passed the criteria specified in Section 6.0 of IPC/JEDEC J-STD-020E, therefore the conclusion of this qualification testing is that our PHEMT2 wafer process is qualified to a moisture/reflow sensitivity classification level of MSL1 per the IPC/JEDEC J-STD-020E.
### Package Ass’y, ESD Classification Level Testing

Samples from four different P/N’s were subjected to testing per Method 3015 of MIL-STD-883 to determine their Electrostatic Discharge Sensitivity Classification. The devices were stabilized at room temperature prior to, and during testing. ESD simulator charging voltages were applied to the devices per the information detailed below.

#### Human Body Model (HBM)

All tests were performed at \( T_A = 25°C \)

<table>
<thead>
<tr>
<th>No. of Samples Tested</th>
<th>Applied ESD Simulator charging voltage ((V_S))</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>&lt; 125V, Class 0A</td>
</tr>
<tr>
<td>5</td>
<td>125V to &lt; 250V, Class 0B</td>
</tr>
<tr>
<td>5</td>
<td>250V to &lt; 500V, Class 1A</td>
</tr>
</tbody>
</table>

![Current Waveform Diagram](image)

The test results show that no degradation in electrical performance was seen following the ESD Sensitivity Classification testing per MIL-STD-883, Method 3015. All material has successfully passed the requirements necessary for a Classification Level 1A rating.
# Process Qualification Report

**CMDS PHEMT2 Wafer Process**

## PHEMT2 Process Qualification Tests & Results Table

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Vehicle</th>
<th>QTY</th>
<th>Test Condition</th>
<th>Inspection</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Temperature Unbiased Bake</td>
<td>Wafer/PCM</td>
<td>210</td>
<td>Ta = 275°C, Duration = 168 hours</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>Autoclave</td>
<td>Wafer/PCM</td>
<td>210</td>
<td>Ta = 121°C, RH = 100%, PSIA = 15, Duration = 96 hours</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>Temperature Cycle</td>
<td>Wafer/PCM</td>
<td>210</td>
<td>-40°C to +125°C, 500 cycles</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>HTOL</td>
<td>Foundry SEC</td>
<td>30</td>
<td>Tj = 255°C, 270°C, &amp; 285°C Ids = 40mA Vds = 3.0 Vdc</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>HTOL (MTTF)</td>
<td>Foundry SMT Device</td>
<td>154</td>
<td>Tj = 150°C, Duration = 1000 hours</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>HTOL</td>
<td>CMD193</td>
<td>92</td>
<td>Tj = 150°C, Duration = 1000 hours</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>Bond Pull</td>
<td>CMD193</td>
<td>10</td>
<td>MIL-STD-883, Method 2011, Condition C</td>
<td>Mechanical</td>
<td>Passed</td>
</tr>
<tr>
<td>Die Shear</td>
<td>CMD193</td>
<td>10</td>
<td>MIL-STD-883, Method 2019</td>
<td>Mechanical</td>
<td>Passed</td>
</tr>
<tr>
<td>Metal Thickness</td>
<td>CMD193</td>
<td>10</td>
<td>Cross-Sectioned, Polished, and Measured</td>
<td>Mechanical</td>
<td>Passed</td>
</tr>
<tr>
<td>SEM Inspection</td>
<td>CMD193</td>
<td>10</td>
<td>MIL-STD-883, Method 2018</td>
<td>Mechanical</td>
<td>Passed</td>
</tr>
</tbody>
</table>
**Process Qualification Report**

**CMDS PHEMT2 Wafer Process**

**Conclusions**

All material passed the screening identified in the table above. The conclusion of this process qualification report is that our PHEMT2 GaAs wafer process is qualified to the specified environmental tests.

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**PHEMT2 Process Qualification Tests & Results Table, cont’d**

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Vehicle</th>
<th>QTY</th>
<th>Test Condition</th>
<th>Inspection</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTOL</td>
<td>CMD132P3</td>
<td>80</td>
<td>Tj = 150°C, Vds = 3.6 Vdc, Duration = 1000 hours</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>Autoclave</td>
<td>CMD132P3</td>
<td>77</td>
<td>Ta = 121°C, RH = 100%, PSIA = 29.7, Duration = 96 hours</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>HAST</td>
<td>CMD132P3</td>
<td>80</td>
<td>Ta = 130°C, RH = 85%, Vds = 3.6 Vdc, Duration = 96 hours</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>Temperature Cycle</td>
<td>CMD132P3</td>
<td>77</td>
<td>-40°C to +125°C, 1000 cycles</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>Thermal Cycle</td>
<td>CMD132P3</td>
<td>77</td>
<td>-40°C to +125°C, 15 minute dwells, 100 cycles</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>Moisture Sensitivity</td>
<td>QFN 4mm x 4mm 24 leads</td>
<td>53</td>
<td>24 hour bake @ 125°C, 168 hours @ 85°C &amp; 85% RH, 3X Reflow at 235°C</td>
<td>CSAM, Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>Moisture Sensitivity</td>
<td>QFN 3mm x 3mm 16 leads</td>
<td>33</td>
<td>24 hour bake @ 125°C, 168 hours @ 85°C &amp; 85% RH, 3X Reflow at 235°C</td>
<td>CSAM, Electrical</td>
<td>Passed</td>
</tr>
<tr>
<td>ESD Classification</td>
<td>Multiple P/N’s</td>
<td>20</td>
<td>Per MIL-STD-883, Method 3015 Class 1A, 499 volts</td>
<td>Electrical</td>
<td>Passed</td>
</tr>
</tbody>
</table>