Process Qualification Report

CMDS PHEMT10 GaAs Wafer Process

Introduction

The definition of a qualification family, as defined by EIA/JESD47 Stress Driven Qualification of Integrated Circuits, is all devices that use the same wafer fabrication technology, wafer fabrication process and wafer fabrication site. This qualification report will outline the screening that was performed to satisfy the reliability requirements for a GaAs MMIC device using Custom MMIC’s PHEMT10 wafer processes.

CMDS offers GaAs PHEMT technology to its customers for RF and Microwave applications. Custom MMIC’s PHEMT10 process consists of an epitaxial structure grown on top of a GaAs wafer to form the active device and semiconductor resistors, as well as numerous passive elements formed in the microelectronic fabrication process.

Qualification testing will consist of the following;

- High Temperature Operating Life (HTOL): SEC1
- High Temperature Storage Test: SEC1
- Temperature Cycle: SEC1
- MTTF Test: SEC1
- Biased Highly Accelerated Temperature/Humidity Stress Test (bHAST): SEC2
- Time Dependent Dielectric Breakdown Test (TDDB): SEC 3
- ESD Classification: SEC4, CMD270P3

Product List

The products listed below are fabricated on the CMDS PHEMT10 GaAs Wafer Process. This Qualification Report is applicable to the following part numbers;

- CMD270
- CMD270P3
- CMD283
- CMD283C3
- CMD295
- CMD295C4
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**Products Selected**

All screening identified as die level was performed on foundry Standard Evaluation Circuits (SEC). The SEC identified as SEC1 is a 100 μm substrate transistor operating at a maximum drain bias of 4.0 volts. SEC2 is a capacitor array of 19 capacitors with areas from 1500 μm² to 48800 μm². SEC3 is a standard MIM capacitor. SEC4 consists of a grouping of PN diodes ranging in size from 20 μm x 5 μm to 100 μm x 5 μm.

Package level screening was performed on the CMD270P3. The CMD270P3 is a broadband MMIC low noise amplifier housed in a leadless 3x3 mm plastic surface mount package. The CMD270P3 is ideally suited for EW and communications systems where small size and low power consumption are needed. The broadband device delivers greater than 16 dB of gain with a corresponding output 1 dB compression point of +18 dBm and a noise figure of 1.7 dB. The CMD270P3 is a 50 ohm matched design eliminating the need for external DC blocks and RF port matching.

Please refer to our product datasheets for detailed device information.
Forty five transistors from three different lots were selected to go through the HTOL reliability testing. The sample structures were biased at 4.0 volts, with the drain current set for 20 mA, and subjected to an ambient temperature of 165°C for 500 hours. The resultant junction temperature was calculated to be 241°C. The failure criteria was selected to be > 20% degradation in \( I_{d_{\text{max}}} \) at the conclusion of the test.

- The maximum degradation in \( I_{d_{\text{max}}} \) was less than 20% after the 500 hours.
- No failures were observed across the entire sample of 135 transistors.

Twenty-two transistors were subjected to 48 hours in a standard oven at a temperature of 250°C. Threshold voltage is measured before thermal exposure, at the 24 hour point, and then again at the conclusion of the testing. The failure criteria was selected to be > 20% degradation in \( V_{t_{\text{on}}} \) at the conclusion of the test.

- The maximum degradation in \( V_{t_{\text{on}}} \) was less than 20% after the 48 hours.

One group of 22 transistors were subjected to thermal cycling testing. The transistors were cycled from –45°C to 125°C using a 15 minute dwell time at temperature, a transition time of less than 5 minutes, and for 1000 cycles. The active parameters are measured prior to the thermal cycle, at 250 cycles, 500 cycles, and at the conclusion of the testing.

- Minimal variation was seen in the critical device characteristics at the conclusion of the thermal cycle test indicating a stable process.

MTTF is a method to evaluate a devices’ long-term reliability when operated at a junction temperature of 125°C. Three lots of 30 transistors were biased at 4.5 volts and a drain current of 40 mA. Each lot is stored at different ambient temperatures until all devices exhibit failure. The ambient temperatures of 150°C, 165°C, and 180°C predict a junction temperature of 289°C, 307°C, and 325°C respectively.

Devices from each junction temperature are continually monitored and the time required for 10%, 50%, and 90% of the devices to reach failure is then recorded. A regression analysis is performed to calculate the 50% failure rate at a Tj of 125°C. The failure criteria was selected to be > 20% degradation in \( I_{d_{\text{max}}} \).

- An MTTF of 2.55x10^8 hours at a Tj 125°C was calculated.
- An activation energy of 1.50eV was also determined.
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SEC1, Biased Highly Accelerated Temperature/Humidity Stress Test, (bHAST)

Bias HAST is a test used to evaluate how well an electronic component resists moisture ingestion. A total of 240 transistors from three different process lots were selected for bHAST screening. The samples were mounted to a test board and biased at a Vd of 4.0 volts and a Vg of 0 volts. The biased samples were then subjected to a temperature of 130°C with a relative humidity of 85% and pressurized to 33.3 psia for a duration of 96 hours.

Transistor Vto and gate leakage were measured prior to screening and at the completion of the 96 hours. The failure criteria of greater than a 20% change in Vto, and a gate leakage of more than 1 mA/mm at the conclusion of the 96 hours was determined.

◊ All 240 samples passed the criteria established above of < 20% change in Vto and < 1 mA/mm gate leakage.

SEC2, Biased Highly Accelerated Temperature/Humidity Stress Test, (bHAST)

To evaluate how well the PHEMT10 capacitor configuration resists moisture ingestion, 400 capacitor array samples from five different process lots were selected for bHAST screening. The samples were mounted to a test board and biased at 8.0 volts. The biased samples were then subjected to a temperature of 130°C with a relative humidity of 85% and pressurized to 33.3 psia for a duration of 96 hours.

Capacitor leakage was measured prior to screening and at the completion of the 96 hours. The failure criteria of greater than a leakage of more than 100 µA at the conclusion of the 96 hours was determined.

◊ One capacitor array failed at the completion of the 96 hours. The remaining 399 arrays passed the criteria established above of < 100 µA for capacitor leakage.
◊ One failure at 96 hours equates to a 0.25% yield fallout.

SEC3, Time Dependent Dielectric Breakdown, (TDDB)

TDDB is a method to evaluate a capacitor’s long-term reliability when operated at an ambient temperature of 125°C, and a 20 volt bias. Ten capacitors are biased at different voltages at the same 125°C ambient temperature until the capacitors exhibit catastrophic failure. The observed time required for each capacitor to reach failure is then used in a regression analysis to calculate the TDDB at 125°C ambient temperature under a 20 volt bias condition.

◊ The TDDB results have been calculated at 1.15E11 seconds or 182 years of bias at 20 volts at an ambient temperature of 125°C.
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CMD270P3 & SEC4, ESD Classification Level Testing

The human-body model (HBM) electro-static discharge test is used to characterize how susceptible an electronic device is to damage from an electro-static discharge (ESD). Multiple PN diode of various sizes were subjected to an ESD of 500 volts for a 20 µm x 5 µm device up to 3000 volts for a 100 µm x 5 µm device. CMD270P3 sample devices were subjected to an ESD of 150 volts, 250 volts, and 500 volts. The devices were stabilized at room temperature prior to, and during testing. PN diode device failure is defined as a 30% change in reverse voltage after being subjected to the ESD discharge. CMD270P3 failure is defined as performance outside applicable datasheet specification. Maximum discharge voltages that the applicable device survived is identified in the table below.

<table>
<thead>
<tr>
<th>Test Unit</th>
<th>Maximum discharge voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMD270P3</td>
<td>500 volts, Classification 1A</td>
</tr>
<tr>
<td>SEC4, 20 µm x 5 µm</td>
<td>500 volts</td>
</tr>
<tr>
<td>SEC 4, 40 µm x 5 µm</td>
<td>1000 volts</td>
</tr>
<tr>
<td>SEC 4, 60 µm x 5 µm</td>
<td>1700 volts</td>
</tr>
<tr>
<td>SEC 4, 80 µm x 5 µm</td>
<td>2000 volts</td>
</tr>
<tr>
<td>SEC 4, 100 µm x 5 µm</td>
<td>2800 volts</td>
</tr>
</tbody>
</table>

Human Body Model (HBM), current pulse waveform

![Current waveform diagram]

**NOTES:**
1. The current waveforms shown shall be measured as described in the waveform verification procedure of 3.2 using equipment meeting the requirements of 2.
2. The current pulse shall have the following characteristics:
   - \( t_{\text{RI}} \) (rise time) ———— Less than 10 nanoseconds.
   - \( t_{\text{Ri}} \) (delay time) ———— 150 ±20 nanoseconds.
   - \( I_p \) (peak current) ———— Within ±10 percent of the \( I_p \) value shown in table II for the voltage step selected.
   - \( t_{\text{RI}} \) (ringing) ———— The decay shall be smooth, with ringing, break points, double time constants or discontinuities less than 15 percent \( I_p \) maximum, but not observable 100 nanoseconds after start of the pulse.
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PHEMT10 GaAs Process Qualification Tests & Results Table

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Vehicle</th>
<th>Test Condition</th>
<th>Failure Criteria</th>
<th>Inspection</th>
<th>Test Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTOL</td>
<td>SEC1</td>
<td>Tj = 241°C, 500 Vds = 5.0 vdc Duration = 500 hours</td>
<td>&gt; 20% degradation in Id_{max}</td>
<td>Electrical</td>
<td>PASSED</td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>SEC1</td>
<td>Ta = 250°C Duration = 48 hours</td>
<td>&gt; 20% degradation in V_{to}</td>
<td>Electrical</td>
<td>PASSED</td>
</tr>
<tr>
<td>Thermal Cycle</td>
<td>SEC1</td>
<td>Temp Range = -45°C to 125°C Dwell = 15 minute Transition Rate = &lt; 5 minutes Duration = 1000 cycles</td>
<td>Characterization only</td>
<td>Electrical</td>
<td>PASSED</td>
</tr>
<tr>
<td>MTTF</td>
<td>SEC1</td>
<td>Tj = 289°C, 307°C, &amp; 325°C Bias = 4.5vdc &amp; 40 mA</td>
<td>&gt; 20% degradation in Id_{max}</td>
<td>Electrical</td>
<td>PASSED</td>
</tr>
<tr>
<td>bHAST</td>
<td>SEC1</td>
<td>Ta = 130°C RH = 85% Pressure = 33.3 psia Duration = 96 hours</td>
<td>&gt; 20% change in V_{to} &gt; 1 mA/mm gate voltage</td>
<td>Electrical</td>
<td>PASSED</td>
</tr>
<tr>
<td>bHAST</td>
<td>SEC2</td>
<td>Ta = 130°C RH = 85% Pressure = 33.3 psia Duration = 96 hours</td>
<td>&gt; 20% change in V_{to} &gt; 1 mA/mm gate voltage</td>
<td>Electrical</td>
<td>PASSED</td>
</tr>
<tr>
<td>TDDB</td>
<td>SEC3</td>
<td>Ta = 125°C</td>
<td>Characterization only</td>
<td>Electrical</td>
<td>PASSED</td>
</tr>
<tr>
<td>ESD Classification</td>
<td>SEC4</td>
<td>500 volts to 3000 volts</td>
<td>&gt; 30 % change in Reverse Voltage</td>
<td>Electrical</td>
<td>PASSED</td>
</tr>
<tr>
<td>ESD Classification</td>
<td>CMD270P3</td>
<td>Class 1A per MIL-STD-883, Method 3015, 500Volts.</td>
<td>Datasheet Parameters</td>
<td>Electrical</td>
<td>PASSED</td>
</tr>
</tbody>
</table>

Conclusion

Custom MMIC has completed the characterization and qualification of our PHEMT10 GaAs wafer fabrication process according to internal procedures and industry standard practices. All test data and results meets or exceeds the required internal criteria identified in the Table above.

The conclusion of this reliability screening is that our PHEMT10 GaAs wafer process is qualified to the specified environmental tests and approved for full production release.

Please note, all information contained in this report is subject to change without notice.