



Process Qualification Report

CMD5 HBT1 & HBT2 InGaP Wafer Process

QUALIFICATION TEST REPORT

Wafer Process: HBT1 & HBT2

Drawing No.: 102578

CMD177	CMD251
CMD177C3	CMD251C3
CMD178	CMD252C4
CMD178C3	CMD253C3
CMD179	CMD254C3
CMD179C3	CMD255C3
CMD180C3	CMD256
CMD181	CMD257
CMD182	CMD257C4
CMD182C4	CMD258C4
CMD183C4	CMD261
CMD225	
CMD225C3	
CMD226	
CMD226C3	
CMD227	
CMD227C3	
CMD245	
CMD245C4	
CMD246	
CMD246C4	
CMD247	
CMD247P4	

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Introduction

CMDS offers GaAs based InGaP HBT technology to its customers for RF and Microwave applications. Currently two processes that use different starting epi structures have been qualified and used in production. Both processes share the same process modules with the only difference being in epitaxy structures. In terms of active devices, each of these processes have to be qualified separately due to the difference in epi structures and device bias conditions. The passive elements and interconnections of these processes share the same physical structures, design rules, and process flow, therefore the qualification of the passive structures has been applied to both processes. The scope of this report will focus on the qualification of the active structures of both processes.

The CMDS HBT Process is a power HBT process, and the process that has been used for the baseline qualification purpose. The CMDS HBT1 & HBT2 are slight modifications to the HBT process.

The definition of a qualification family, as defined by EIA/JESD47 Stress Driven Qualification of Integrated Circuits, is all devices that use the same wafer fabrication technology, wafer fabrication process and wafer fabrication site. This qualification report will outline the screening that was performed to satisfy the reliability requirements for a GaAs MMIC device using Custom MMIC's HBT1 & HBT2 InGaP wafer processes.

All screening identified as die level was performed on foundry Standard Evaluation Circuits (SEC). The SEC identified as HBT is the evaluation circuit used to qualify the baseline process. The SEC's identified as HBT1 & HBT2 are devices with differences in epitaxy structure and bias conditions, and will therefore be subjected to individual HTOL screening.

Qualification testing will consist of the following:

- ◇ High Temperature Operating Life (HTOL): HBT, HBT1, & HBT2 SEC's
- ◇ High Temperature Storage Test: HBT SEC
- ◇ Humidity/Temperature Test (HAST): HBT SEC
- ◇ MSL Screening: Packaged devices
- ◇ ESD Classification: Packaged devices



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Products Selected

All screening identified as die level was performed on foundry Standard Evaluation Circuits (SEC). The SEC identified as HBT is the baseline process. The SEC's identified as HBT1 and HBT2 are slight modifications to the baseline process. The HBT SEC was selected for the majority of the screening, and the HBT1 & HBT2 SEC's were included in HTOL screening.

The HBT SEC is a 2x2x6um cell with bias conditions of $J_c=50\text{kA/cm}^2$ and $V_{ce}=3$ to 3.6 volts. The HBT1 SEC is a 2x6x2um cell with bias conditions of $J_c=50\text{kA/cm}^2$ and $V_{ce}=3$ to 3.6 volts. The HBT2 SEC is a 1.6x4um² cell with bias conditions of $J_c=200\text{kA/cm}^2$.

All screening identified as package level was performed on the CMD245C4 for the HBT1 process, and the CMD177C3 for the HBT2 process.

The CMD245C4 is a wideband GaAs MMIC low phase noise amplifier housed in a leadless surface mount package that is ideally suited for military, space and communications systems. At 10 GHz the device delivers 18 dB of gain, a saturated output power of +21 dBm and a noise figure of 4.5 dB. Also with an input signal of 10 GHz the amplifier provides low phase noise performance of -165 dBc/Hz at 10 kHz offset. The CMD245C4 is a 50 ohm matched design which eliminates the need for RF port matching.

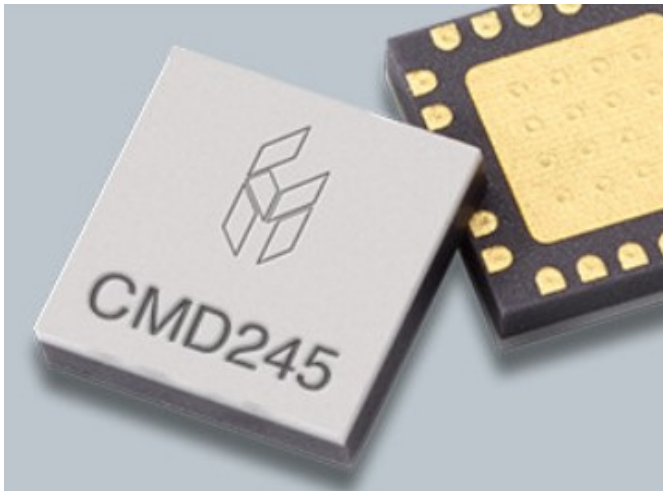
The CMD177C3 is a general purpose double balanced mixer in a leadless surface mount package that can be used for up- and down converting applications between 6 and 14 GHz. The CMD177C3 has very high isolation to both the RF and IF ports due to the optimized balun structures, and can operate with an LO drive level as low as +9 dBm. The CMD177C3 can easily be configured as an image reject mixer or single sideband modulator with external hybrids and power splitters.

Please refer to our product datasheets for detailed device information.

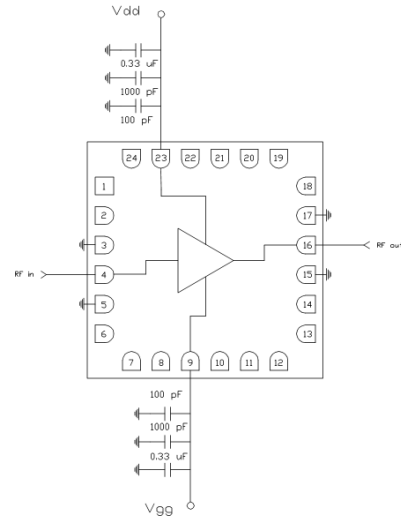
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CMD5 HBT1 & HBT2 Wafer Process

Products Selected, cont'd



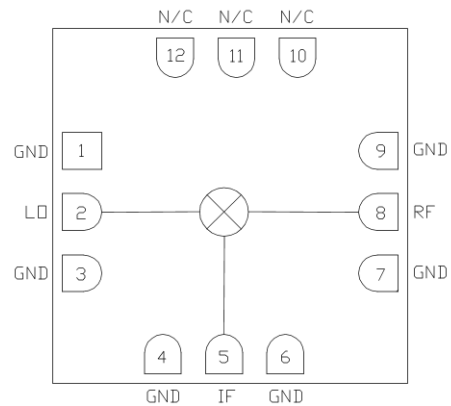
CMD245C4 in a ceramic, air cavity QFN 4x4 mm x 24 lead smt



CMD245C4 Functional Block Diagram



CMD177C3 in a ceramic, air cavity QFN 3x3 mm x 12 lead smt



CMD177C3 Functional Block Diagram



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CMDS HBT1 & HBT2 InGaP Wafer Process

HBT, High Temperature Operating Life, (HTOL)

Three separate HBT lots were selected to go through the HTOL reliability testing. 30 samples from each of the 3 lots were separated into 3 groups of 10 each and subjected to bias stress conditions at 3 different junction temperatures. The failure criteria was selected to be 20% degradation in dc current from the one hour data reference point.

The first group of 10 devices from each of the 3 lots were subjected to a T_j of 253°C and a bias condition of 3.0vdc. The second group of 10 devices from each of the 3 lots were subjected to a T_j of 272°C and a bias condition of 3.6vdc. The last group of 10 devices from each of the 3 lots were subjected to a T_j of 295°C and a bias condition of 3.6vdc.

- ◇ The deduced Activation energy for all 3 lots was 1.14eV.
- ◇ The projected MTTF at a T_j of 125°C is 8e6 hours.

HBT1, High Temperature Operating Life, (HTOL)

Three separate HBT1 lots were selected to go through the HTOL reliability testing. 30 samples from each of 3 different wafer lots were subjected to bias stress conditions at 3 different junction temperatures. The failure criteria was selected to be 20% degradation in dc current from the one hour data reference point.

The first group of 10 devices from each of the 3 lots were subjected to a T_j of 257°C and a bias condition of 3.0vdc. The second group of 10 devices from each of the 3 lots were subjected to a T_j of 275°C and a bias condition of 3.6vdc. The last group of 10 devices from each of the 3 lots were subjected to a T_j of 300°C and a bias condition of 3.6vdc.

- ◇ The deduced Activation energy for all 3 lots was 1.09eV.
- ◇ The projected MTTF at a T_j of 125C is 2.8e9 hours.

HBT2, High Temperature Operating Life, (HTOL)

One group of twenty devices was subjected to a bias condition of 12.8 mA/diode (200KA/cm²) and a T_j of 257°C for 1000 hours. The failure criteria was selected to be a 20% change in dynamic @ 12.8 mA.

The twenty devices were tested at the conclusion of the 1000 hours and there were no changes in device characteristics.



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HBT, High Temperature Storage Test

One group of 68 HBT devices were randomly selected from a production wafer and separated into two lots of 34 devices each. The first lot of 34 devices was subjected to a high temperature storage of 225°C. The second lot of 34 devices was subjected to a high temperature storage of 225°C. The duration for each high temperature storage test was 1000 hours. The dc current was monitored during the test and remained stable with no noticeable degradation.

HBT, Biased Humidity and Temperature Test

Two separate humidity tests were conducted according to JEDEC standards. The first is the Steady State Temperature Humidity Bias Life per JESD22-A101. The second test is the Cycled Temperature Humidity Bias Life Test per JESD22-A100. Two groups of 10 HBT devices each were randomly selected and subjected to the above referenced testing.

In the steady state temperature test, the ambient temperature was 85°C and the relative humidity was 85%. The bias condition during this test was 3 volts and 100 μ A. The total test duration was 1198 hours.

In the cycled temperature test, the temperature was cycled between 30°C and 65°C. The relative humidity was 94%. The bias condition during this test was 3 volts and 100 μ A. The total test duration was 1030 hours.

All material was measured prior to, and following the HAST test per the screening identified above. No changes in device characteristics were seen.

Package Ass'y, Moisture Sensitivity Level Classification

Material samples from 2 non-consecutive build lots were electrically tested before and after being subjected to the procedure specified in J-STD-020E, classification level MSL1. Visual inspection and acoustic microscope inspection (CSAM) was performed before and after moisture soak and reflow per MSL1 levels specified by IPC/JEDEC J-STD-020E. No degradation in product performance was seen.

All material passed the criteria specified in Section 6.0 of IPC/JEDEC J-STD-020E, therefore the conclusion of this qualification testing is that our QFN ceramic air cavity surface mount package style is qualified to a moisture/reflow sensitivity classification level of MSL1 per the IPC/JEDEC J-STD-020E.

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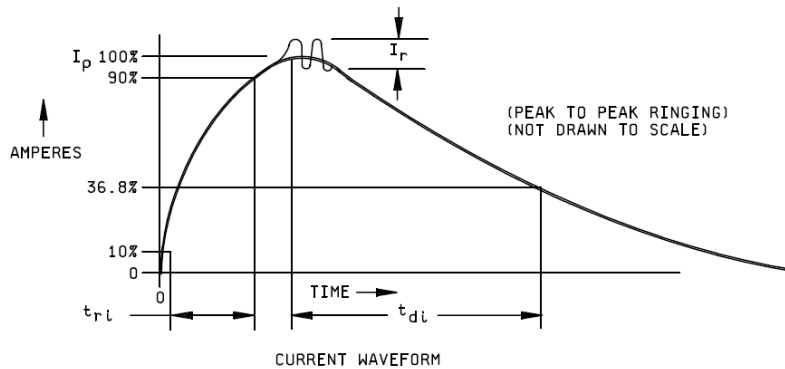
Package Ass'y, ESD Classification Level Testing

Samples from each of the 5 different P/N's were subjected to testing per Method 3015 of MIL-STD-883 to determine their Electrostatic Discharge Sensitivity Classification. The devices were stabilized at room temperature prior to, and during testing. ESD simulator charging voltages were applied to the devices per the information detailed below.

Human Body Model (HBM)

All tests were performed at $T_A=25^\circ\text{C}$

No. of Samples Tested	Applied ESD Simulator charging voltage (V_S)
5	< 125V, Class 0A
5	125V to < 250V, Class 0B
5	250V to < 500V, Class 1A



NOTES:

- The current waveforms shown shall be measured as described in the waveform verification procedure of 3.2, using equipment meeting the requirements of 2.
- The current pulse shall have the following characteristics:

T_{ri} (rise time)Less than 10 nanoseconds.
 T_{di} (delay time).....150 \pm 20 nanoseconds.
 I_p (peak current).....Within \pm 10 percent of the I_p value shown in table II for the voltage step selected.
 I_r (ringing)The decay shall be smooth, with ringing, break points, double time constants or discontinuities less than 15 percent I_p maximum, but not observable 100 nanoseconds after start of the pulse.

The test results show that no degradation in electrical performance was seen following the ESD Sensitivity Classification testing per MIL-STD-883, Method 3015. All material has successfully passed the requirements necessary for a Classification Level 1A rating.



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HBT, HBT1, & HBT2 InGaP Process Qualification Tests & Results Table

Test	Test Vehicle	Test Condition	Failure Criteria	Inspection	Test Results
HTOL	HBT SEC DIE	Tj = 253°C, 272°C, & 295°C Vce = 3.0vdc, 3.0vdc, & 3.6vdc	20% degradation in dc current	Electrical	PASSED
HTOL (1)	HBT1 SEC DIE	Tj = 257°C, 275°C, & 300°C Vce = 3.0vdc, 3.0vdc, & 3.6vdc	20% degradation in dc current	Electrical	PASSED
HTOL (2)	HBT2 SEC DIE	Tj = 230°C, JC = 200kA/cm2 1000 hours	Δ (dynamicR@12.8mA)>20%	Electrical	PASSED
Temperature, Humidity, Bias	HBT SEC DIE	Per JESD22-A101-B, Bias = 3.0vdc & 100uA 85°C & 85% RH for 1198 hours	20% degradation in dc current	Electrical	PASSED
Temperature, Humidity, Bias	HBT SEC DIE	Per JESD22-A100-B, Bias = 3.0vdc & 100uA Temp Cycle: 30°C to 65°C, Humidity: 94% RH Duration: 1198 hours	20% degradation in dc current	Electrical	PASSED
High Temperature Storage	HBT SEC DIE	JESD22-A103, 225°C & 250°C 1000 hours	No changes in device characteristics	Electrical	PASSED
Moisture Sensitivity	QFN 4mm x 4mm 24 leads	24 hour bake @ 125°C Moisture soak: 168 hrs at 85°C & 85% RH 3X Reflow at 235°C	Per J-STD-020E, MSL1	CSAM Electrical	PASSED
Moisture Sensitivity	QFN 3mm x 3mm 12 leads	24 hour bake @ 125°C Moisture soak: 168 hrs at 85°C & 85% RH 3X Reflow at 235°C	Per J-STD-020E, MSL1	CSAM Electrical	PASSED
ESD Classification	QFN 4mm x 4mm 24 leads	Class 1A per MIL-STD-883, Method 3015, 499Volts.	Datasheet Parameters	Electrical	PASSED
ESD Classification	QFN 3mm x 3mm 12 leads	Class 1A per MIL-STD-883, Method 3015, 499Volts.	Datasheet Parameters	Electrical	PASSED

Conclusions

All material passed the criteria specified in the Table above. The conclusion of this reliability screening is that our HBT1 & HBT2 InGaP GaAs wafer processes are qualified to the specified environmental tests.

Please note, all information contained in this report is subject to change without notice.

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