

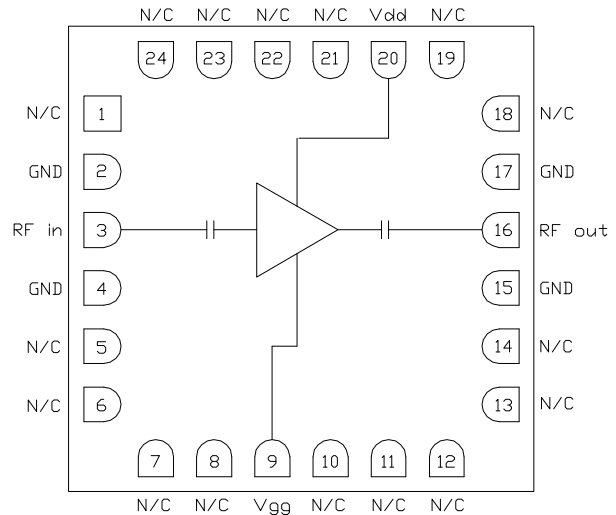
### Features

- ▶ High gain
- ▶ Low noise figure
- ▶ High linearity
- ▶ High RF power survivability
- ▶ Pb-free RoHs compliant 4x4 QFN package

### Description

The CMD218C4 is a broadband MMIC GaN low noise amplifier housed in a leadless 4x4 mm QFN package. The CMD218C4 is ideally suited for microwave radios and C and X-band applications where small size and high input power survivability are needed. The broadband device delivers greater than 22 dB of gain with a corresponding output 1 dB compression point of +18.5 dBm and a noise figure of 1.1 dB. The CMD218C4 features an RF input power survivability of greater than 5 Watts.

### Functional Block Diagram



### Electrical Performance - $V_{dd} = 10\text{ V}$ , $I_{dd} = 75\text{ mA}$ , $T_A = 25\text{ }^\circ\text{C}$ , $F = 7\text{ GHz}$

Parameter	Min	Typ	Max	Units
Frequency Range	5 - 9			GHz
Gain		22		dB
Noise Figure		1.1		dB
Output P1dB		18.5		dBm
Output Psat		26		dBm
Output IP3		29		dBm
Input Return Loss		15		dB
Output Return Loss		10		dB
Supply Current		75		mA



# CMD218C4

## 5-9 GHz GaN Low Noise Amplifier

### Specifications

#### Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, V <sub>dd</sub>	35 V
RF Input Power	5 W Pulsed
Channel Temperature, T <sub>ch</sub>	150 °C
Power Dissipation, P <sub>diss</sub>	3.5 W
Thermal Resistance, $\Theta_{JC}$	18.7 °C/W
Operating Temperature	-40 to 85 °C
Storage Temperature	-55 to 150 °C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

#### Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V <sub>dd</sub>	5	10	28	V
I <sub>dd</sub>		75		mA
V <sub>gg</sub>	-10	-2.3	-1	V

Electrical performance is measured at specific test conditions. Electrical specifications are not guaranteed over all recommended operating conditions.

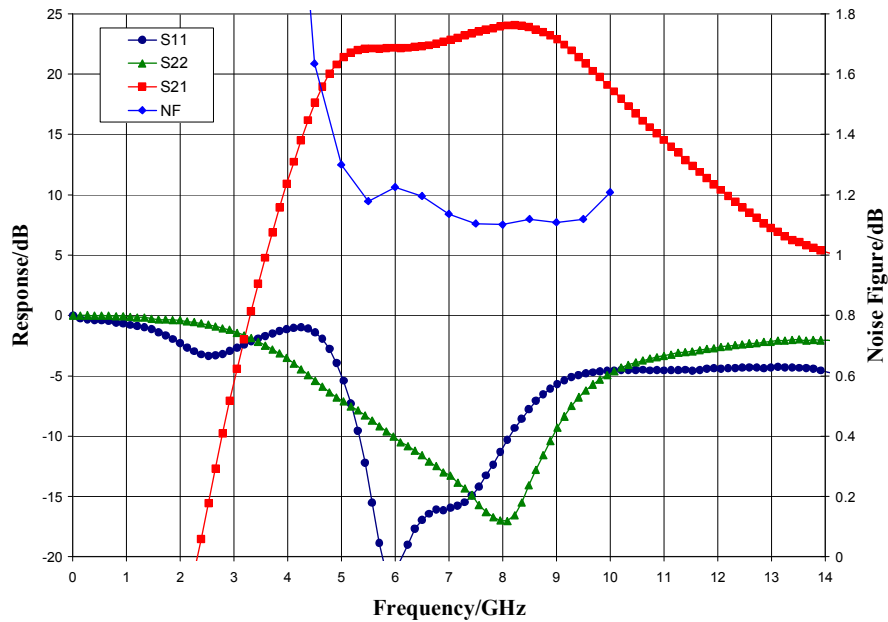
#### Electrical Specifications - V<sub>dd</sub> = 10 V, I<sub>dd</sub> = 75 mA, T<sub>A</sub> = 25 °C

Parameter	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range	5 - 7			7 - 9			GHz
Gain	17	22	27	19	24	28	dB
Noise Figure		1.2	1.7		1.1	1.6	dB
Input Return Loss		13			10		dB
Output Return Loss		8			13		dB
Output P <sub>1dB</sub>		18.5			19.5		dBm
Output IP <sub>3</sub>		29			29.5		dBm
Supply Current	52	75	98	52	75	98	mA
Gain Temperature Coefficient		0.03			0.03		dB/°C
Noise Figure Temperature Coefficient		0.009			0.009		dB/°C

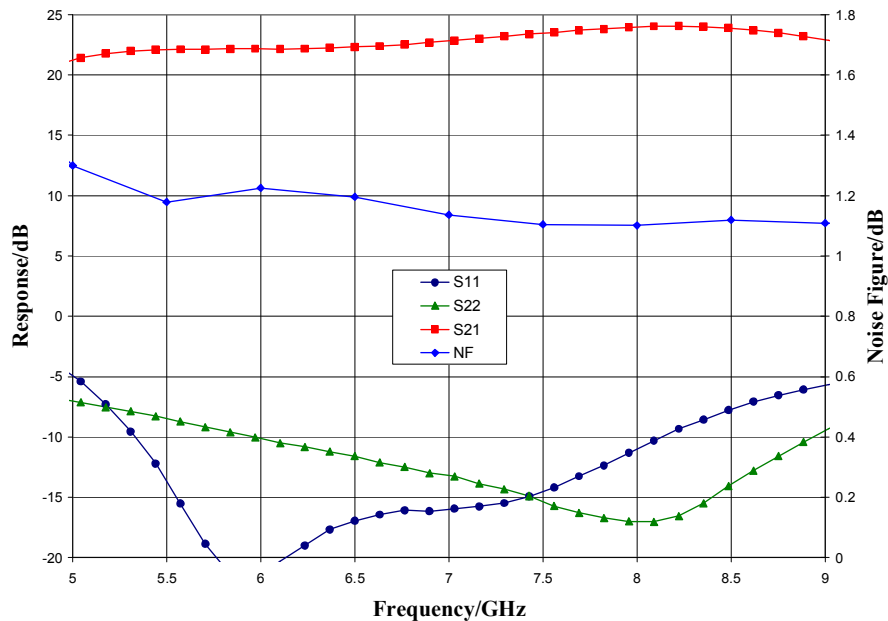
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### Typical Performance

**Broadband Performance,  $V_{dd} = 10\text{ V}$ ,  $I_{dd} = 75\text{ mA}$ ,  $T_A = 25\text{ }^\circ\text{C}$**



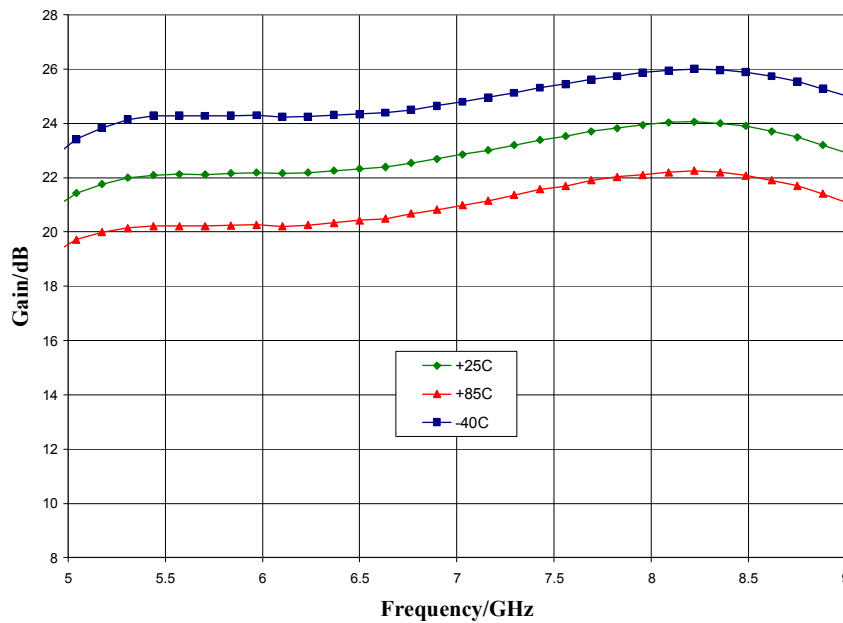
**Narrow-band Performance,  $V_{dd} = 10\text{ V}$ ,  $I_{dd} = 75\text{ mA}$ ,  $T_A = 25\text{ }^\circ\text{C}$**



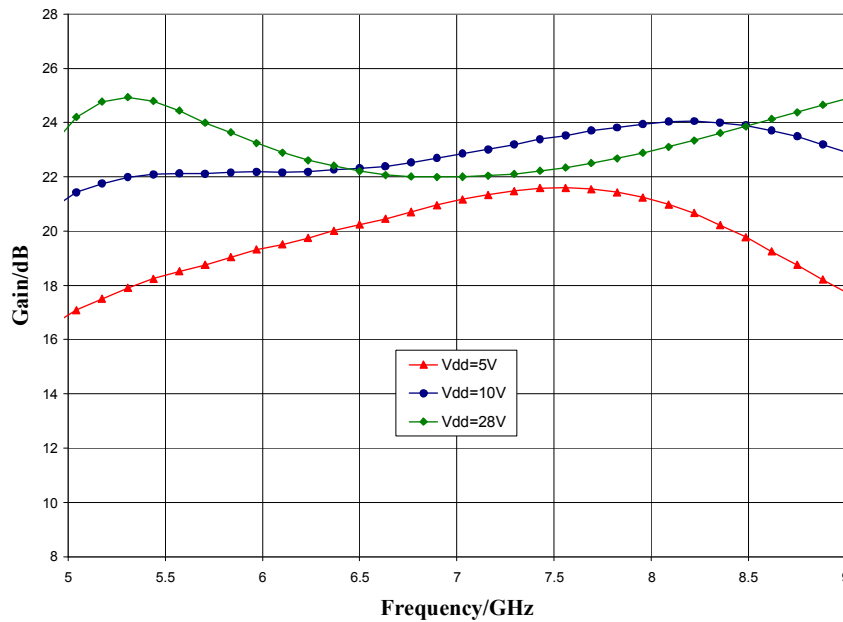
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### Typical Performance

Gain vs. Temperature,  $V_{dd} = 10\text{ V}$

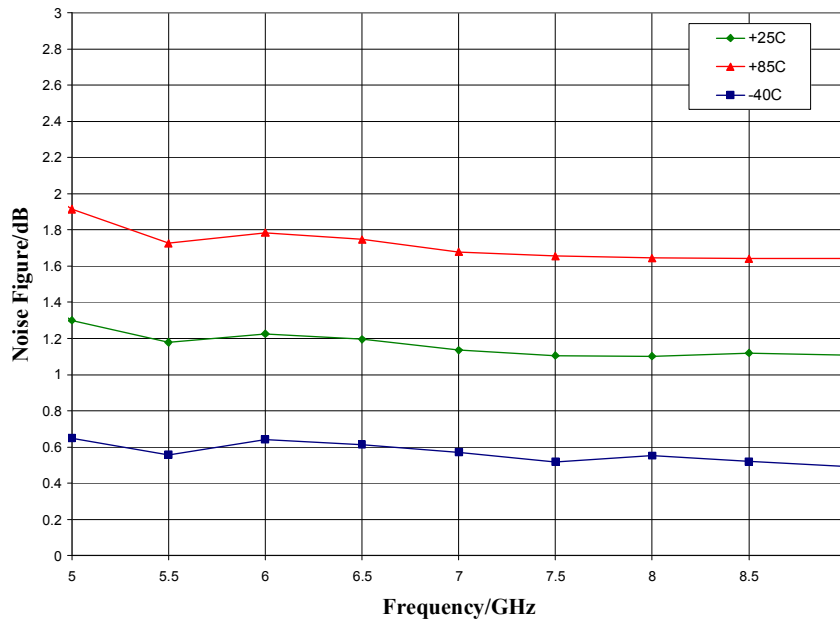


Gain vs.  $V_{dd}$ ,  $I_{dd} = 75\text{ mA}$ ,  $T_A = 25\text{ }^\circ\text{C}$

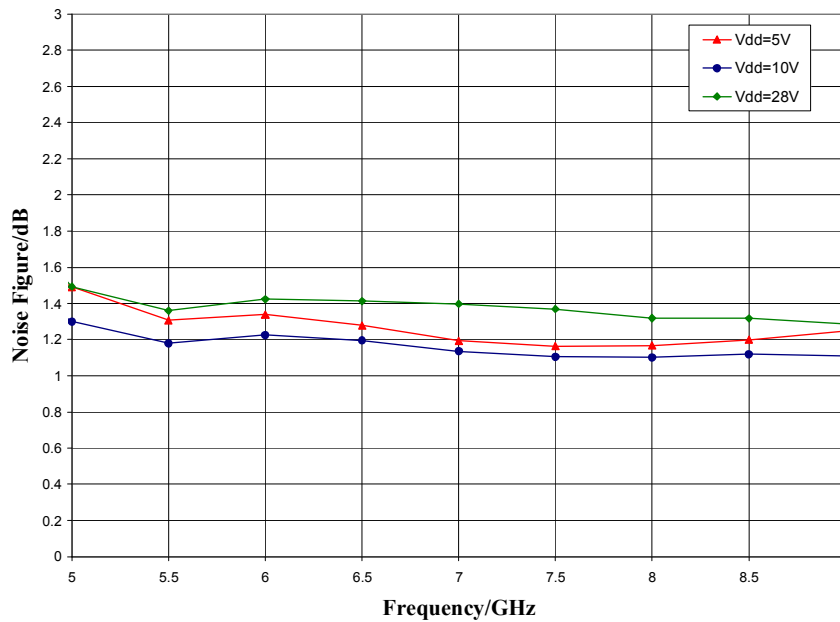


### Typical Performance

Noise Figure vs. Temperature,  $V_{dd} = 10\text{ V}$ ,

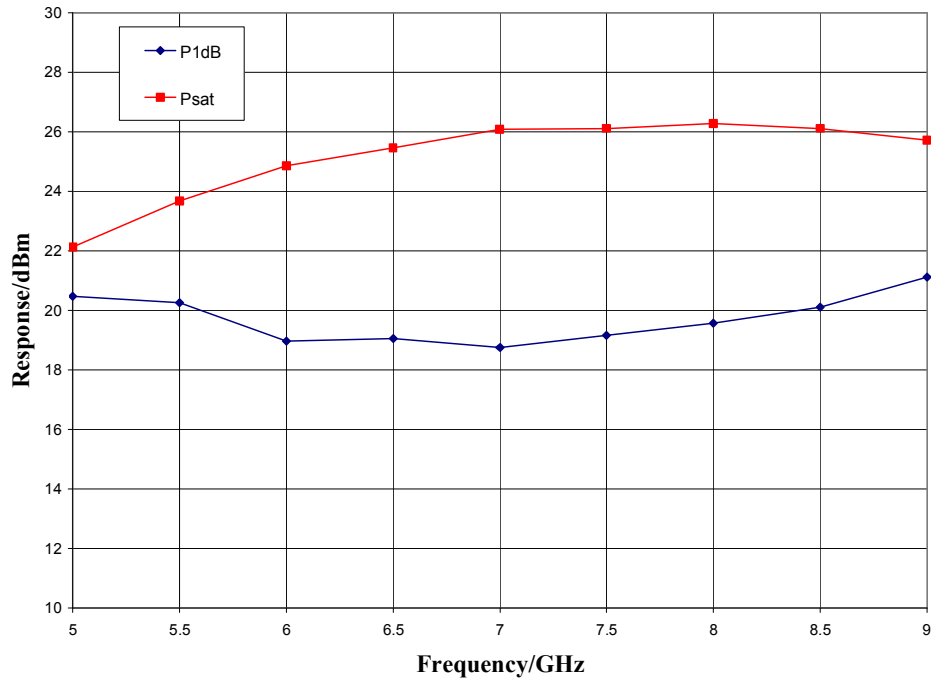


Noise Figure vs.  $V_{dd}$ ,  $I_{dd} = 75\text{ mA}$ ,  $T_A = 25\text{ }^\circ\text{C}$

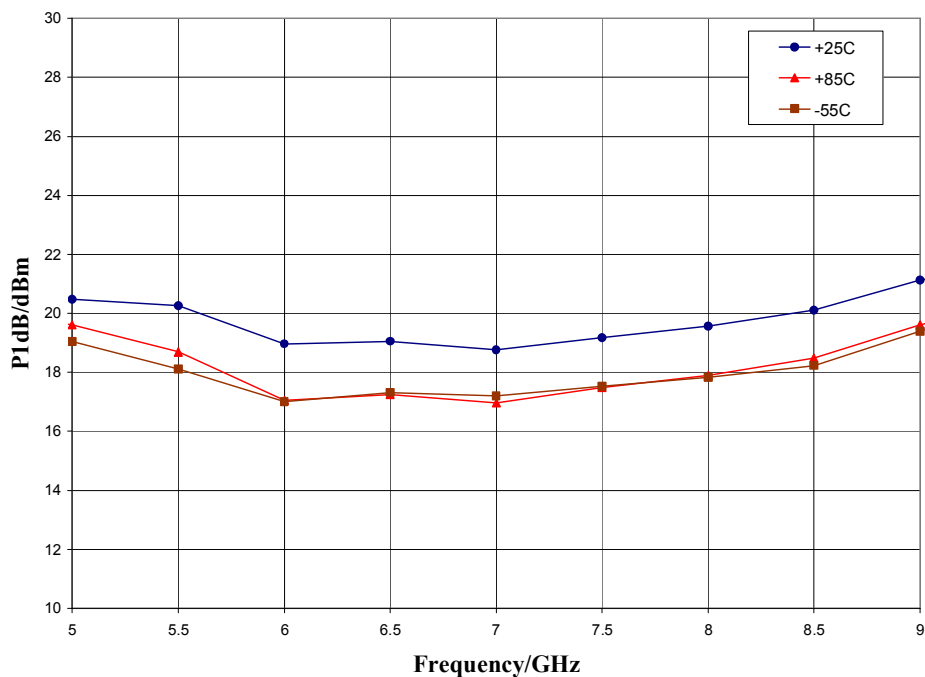


### Typical Performance

Output Power,  $V_{dd} = 10\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$



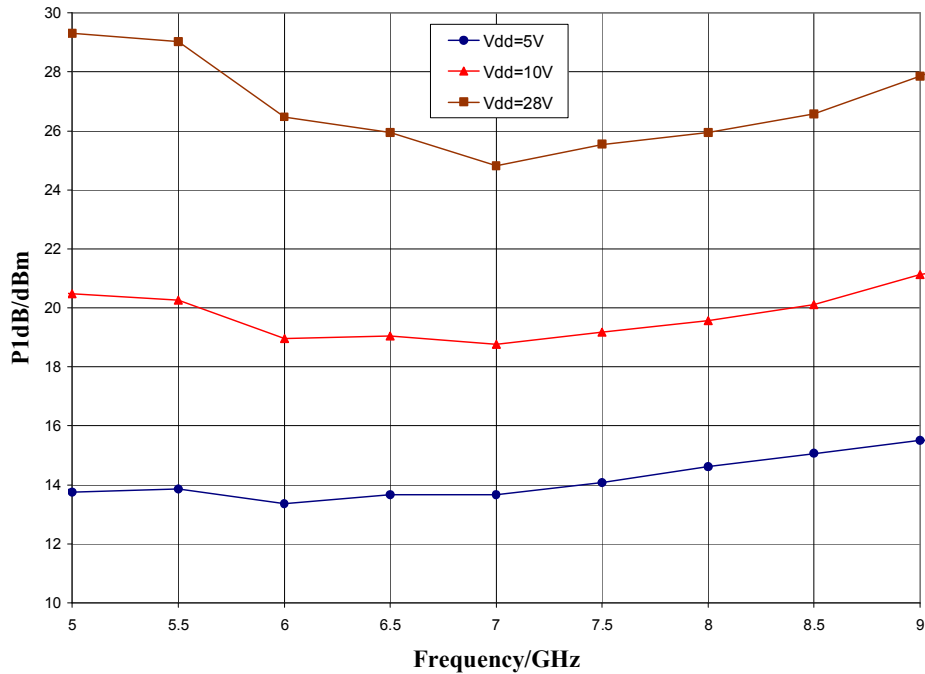
P1dB vs. Temperature,  $V_{dd} = 10\text{ V}$



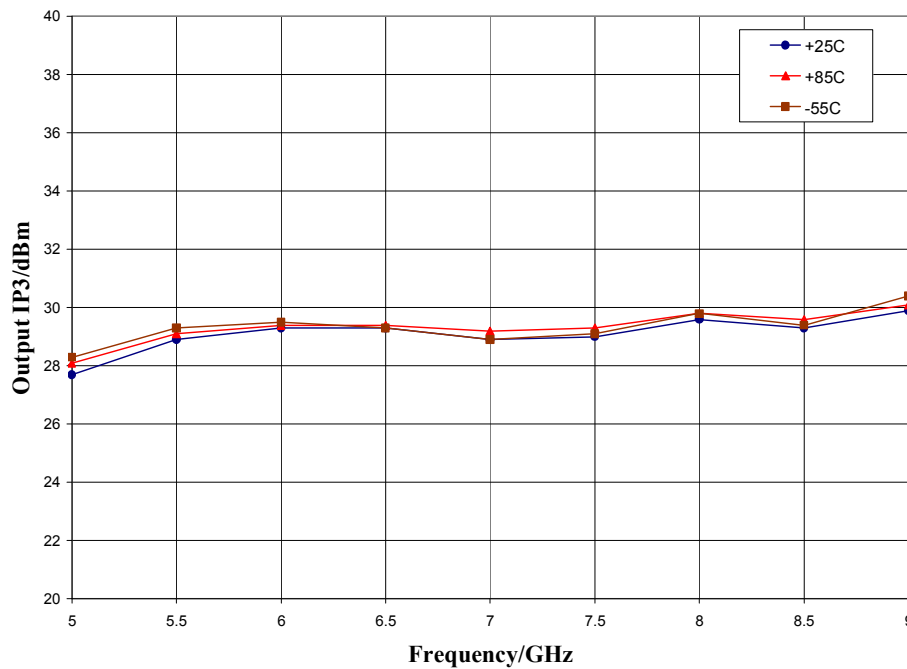
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### Typical Performance

**P1dB vs.  $V_{dd}$ ,  $T_A = 25^\circ\text{C}$**



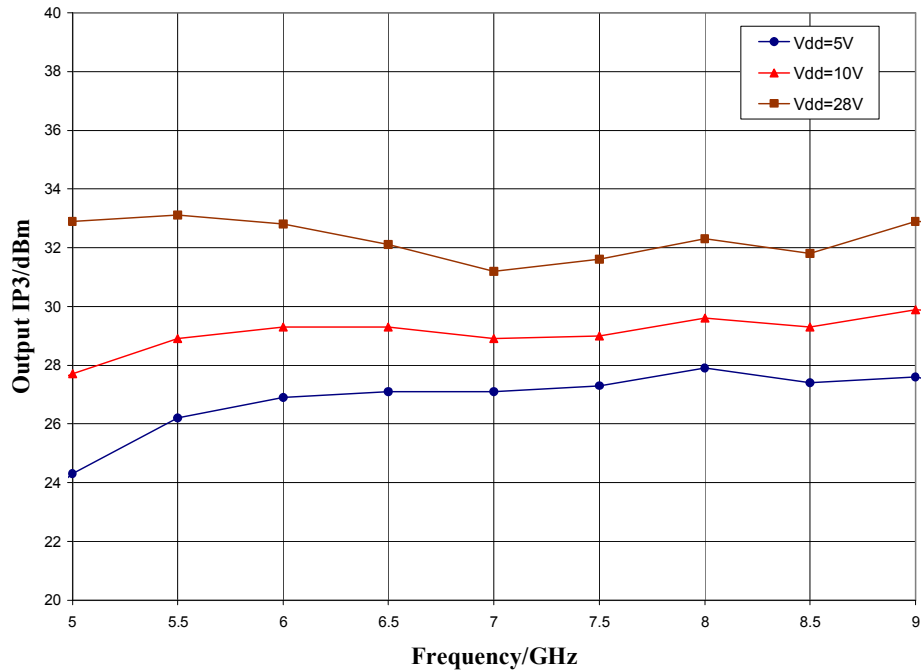
**Output IP3 vs. Temperature,  $V_{dd} = 10\text{ V}$ ,  $I_{dd} = 75\text{ mA}$**



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### Typical Performance

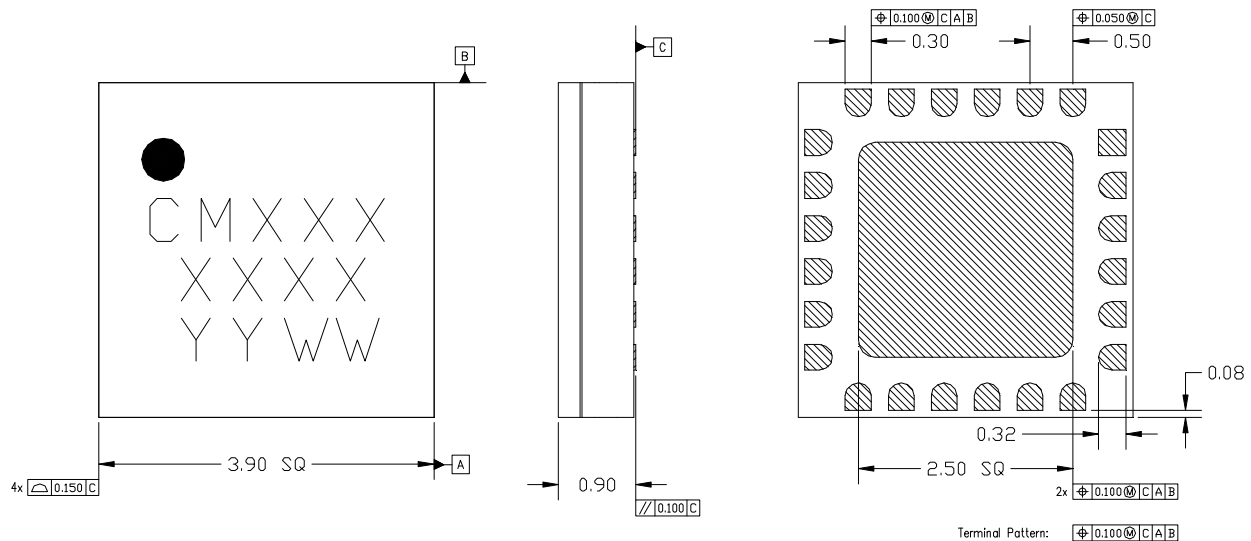
Output IP3 vs.  $V_{dd}$ ,  $I_{dd} = 75 \text{ mA}$ ,  $T_A = 25 \text{ }^\circ\text{C}$





### Mechanical Information

#### Package Information and Dimensions



- NOTES:
1. ALL DIMENSIONS SHOWN IN mm.
  2. MATERIAL: BLACK ALUMINA
  3. LEAD FINISH:
    - 3.1. Ni: 8.89um MAX, 1.27um MIN
    - 3.2. Pd: 0.17um MAX, 0.07um MIN
    - 3.3. Au: 0.254um MAX, 0.03um MIN
  4. MARKING
    - 4.1. LINE 1: PART NUMBER
      - 4.1.1. EXAMPLE: CMD191C4 SHALL BE MARKED AS CM191
    - 4.2. LINE 2: LOT NUMBER
    - 4.3. LINE 3: DATE CODE - LAST 2 DIGITS OF THE YEAR OF MANUFACTURE FOLLOWED BY A 2 DIGIT WEEK CODE
  5. ALTERNATE PIN #1 IDENTIFIER IS A SINGLE SQUARE PAD
  6. ALTERNATE DIE PADDLE MAY HAVE CHAMFERED CORNERS

#### Recommended PCB Land Pattern

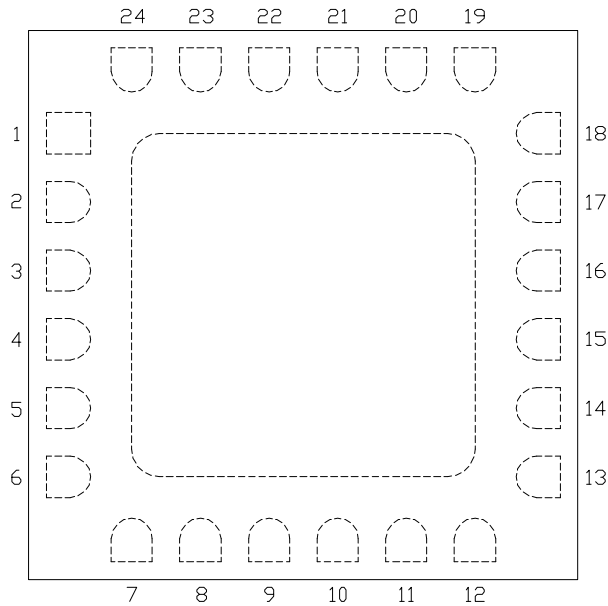
Custom MMIC Design Services recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review Custom MMIC Application Note AN 105 for a recommended land pattern approach.

#### Recommended Solder Reflow Profile


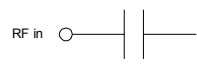
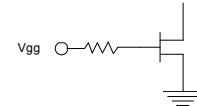

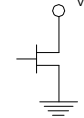
Custom MMIC Design Services recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review Custom MMIC Application Note AN 102 for a recommended solder reflow profile.

### Pin Description

#### Pin Diagram



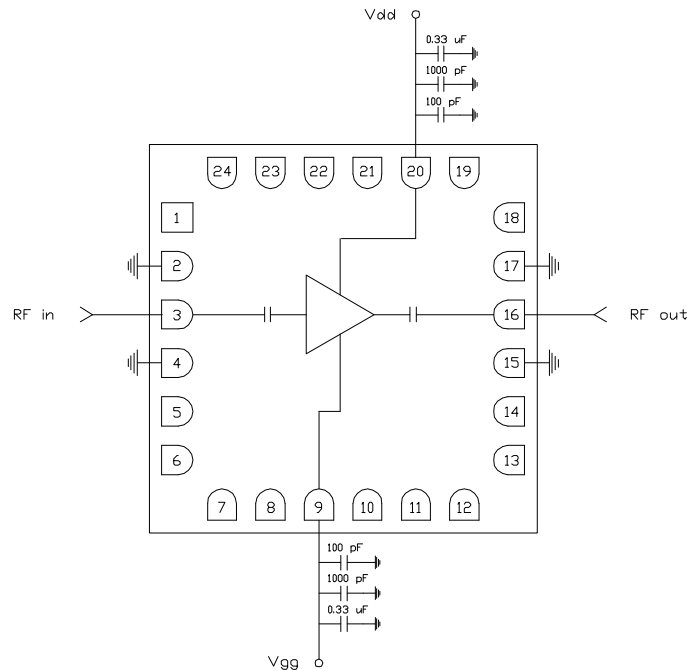
#### Functional Description

Pin	Function	Description	Schematic
1, 5-8, 10-14, 18, 19, 21-24	N/C	No connection required. These pins may be connected to RF/DC ground	
2, 4, 15, 17 and die paddle	Ground	Connect to RF/DC ground	
3	RF in	DC blocked and 50 ohm matched	
9	V <sub>gg</sub>	Power supply voltage Decoupling and bypass caps required	
16	RF out	DC blocked and 50 ohm matched	
20	V <sub>dd</sub>	Power supply voltage Decoupling and bypass caps required	

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### Applications Information

#### Application Circuit



#### Biasing and Operation

The CMD218C4 is biased with a positive drain supply and a negative gate supply. Performance is optimized when the drain voltage is set to +10 V but may be set between +5 V and +28 V.

Turn ON procedure:

1. Apply gate voltage  $V_{gg}$  and set to a voltage sufficient to pinch off drain current ( $\sim -4$  V)
2. Apply drain voltage  $V_{dd}$  and set to +10 V
3. Increase  $V_{gg}$  (less negative) to achieve a drain current of 75 mA

Turn OFF procedure:

1. Turn off drain voltage  $V_{dd}$
2. Turn off gate voltage  $V_{gg}$

RF power can be applied at any time

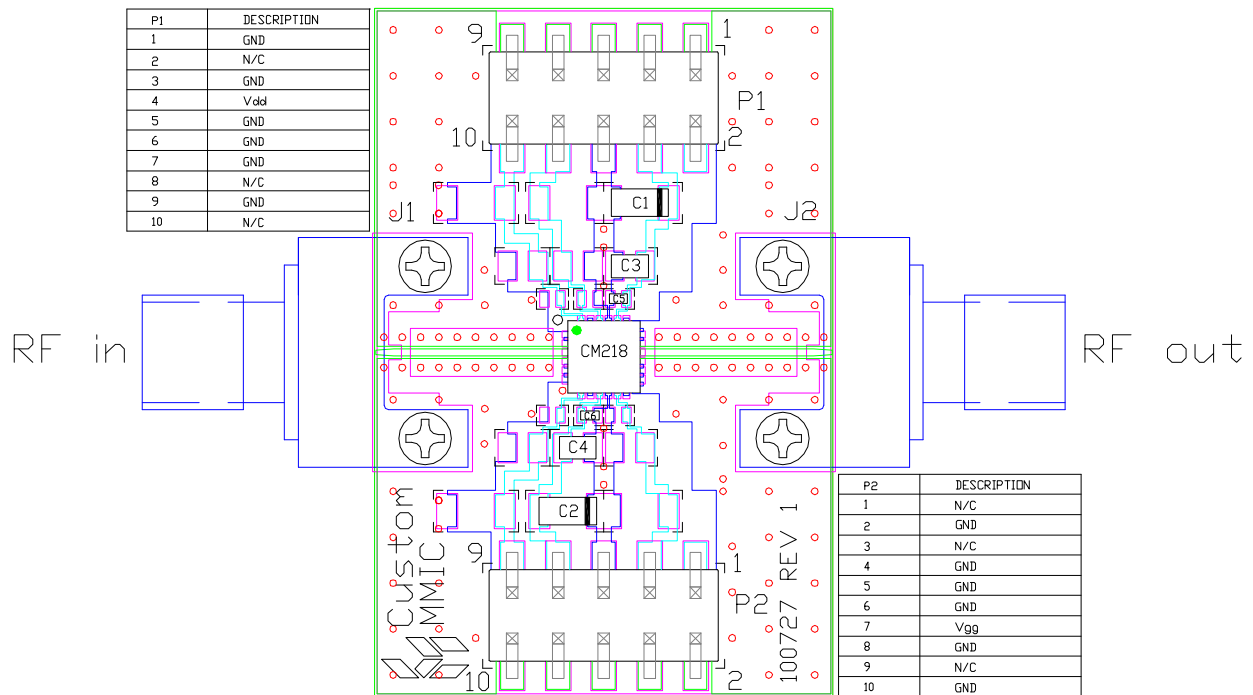
**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

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### Applications Information

#### Evaluation Board

The circuit board shown has been developed for optimized assembly at CMDS. A sufficient number of via holes should be used to connect the top and bottom ground planes. As surface mount processes vary, careful process development is recommended.



Designator	Value	Description
J1, J2		SMA End Launch Connector
P1, P2		10 Pin Header
C1, C2	0.33 $\mu$ F	Capacitor, Tantalum
C3, C4	1000 pF	Capacitor, 0603
C5, C6	100 pF	Capacitor, 0402
U1		CMD218C4 Low Noise Amplifier
PCB		100727 Evaluation PCB

Please note, all information contained in this data sheet is subject to change without notice.

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